

What is claimed is:

1 1. A method of backing up BIOS settings stored in
2 a CMOS memory in a computer system by a DMI memory, the
3 method comprising steps of:

4 executing a power on self test (POST) procedure
5 after powering on the computer system;

6 detecting BIOS settings stored in the CMOS memory;
7 and

8 writing predetermined BIOS settings stored in the
9 DMI memory into the CMOS memory if the BIOS
10 settings stored in the CMOS memory are
11 abnormal.

1 2. The method of claim 1, wherein the computer
2 system subsequently accomplishes the POST procedure if
3 the BIOS settings stored in the CMOS memory are normal.

1 3. The method of claim 1, wherein the BIOS
2 settings are backed up in a memory block of the DMI
3 memory.

1 4. The method of claim 1, wherein the DMI memory
2 is located in a flash memory.

1 5. A method of backing up BIOS settings stored in
2 a CMOS memory in a computer system by a DMI memory, the
3 method comprising the steps of:

4 executing a power on self test (POST) procedure
5 after powering on the computer system;

6 detecting whether the BIOS settings stored in the
7 CMOS memory are normal;

8 determining whether to ignore a reloading function;
9 detecting header data of the DMI memory;
10 determine whether to access the DMI memory according
11 to whether an enabling signal has been set; and
12 writing predetermined BIOS settings stored in the
13 DMI memory into the CMOS memory.

1 6. The method of claim 5, wherein the computer
2 system subsequently accomplishes the POST procedure if
3 the BIOS settings stored in the CMOS memory are normal.

1 7. The method of claim 5, wherein the computer
2 system subsequently accomplishes the POST procedure if
3 the reloading function is ignored.

1 8. The method of claim 5, wherein the computer
2 system subsequently accomplishes the POST procedure if
3 the DMI memory has no header information.

1 9. The method of claim 5, wherein the computer
2 system subsequently accomplishes the POST procedure if
3 the enabling signal is not set.

1 10. The method of claim 5, wherein the BIOS
2 settings are backed up in a memory block of a DMI memory.

1 11. The method of claim 5, wherein the DMI memory
2 is located in a flash memory.

1 12. A method of backing up BIOS settings stored in
2 a CMOS memory in a computer system into a DMI memory,
3 comprising:

4 entering a BIOS setting menu;

5 querying whether BIOS settings being save after
6 exiting the BIOS setting menu;
7 backing up the BIOS settings into the DMI memory.

1 13. The method of claim 12, wherein the BIOS
2 settings are stored in a memory block of the DMI memory.

1 14. The method of claim 12, wherein the DMI memory
2 is located in a flash memory.

1 15. The method of claim 12, wherein the BIOS
2 settings are not saved if saving BIOS settings after
3 exiting the BIOS settings menu is not required.

1 16. A method of backing up a BIOS setting stored in
2 the CMOS memory of a computer system by a DMI memory, the
3 DMI memory including a memory block for storing
4 predetermined BIOS settings in the computer system, the
5 method comprising the following steps:

6 storing the predetermined BIOS settings stored in
7 the CMOS memory to the memory block of the DMI
8 memory;

9 updating the BIOS settings stored in the CMOS memory
10 according to the predetermined BIOS setting
11 stored in the memory block of the DMI memory.

1 17. The method of claim 16, wherein the
2 corresponding memory block of the DMI memory is located
3 in a flash memory.

1 18. The method of claim 16, wherein the CMOS memory
2 is located in a south bridge chipset.

1 19. A computer system for backing up BIOS settings
2 in a memory block of a flash memory, comprising:
3 a central processing unit (CPU);
4 a front side system bus (FSB) for connecting a north
5 bridge chip to the CPU;
6 a double data rate (DDR) memory bus for connecting
7 the north bridge chip to a memory module;
8 an accelerated graphic port (AGP) bus for connecting
9 the north bridge chip to a display card module;
10 a peripheral component interconnect (PCI) bus for
11 connecting a south bridge chip to a plurality
12 of peripheral devices;
13 a CMOS memory located in the south bridge chip; and
14 a flash memory located on a motherboard of the
15 computer system, wherein the flash memory
16 comprises a first memory block for a DMI
17 memory.

1 20. The computer system of claim 19, wherein the
2 BIOS settings are stored in the CMOS memory.

1 21. The computer system of claim 19, wherein the
2 memory block of the flash memory comprises a memory block
3 for the DMI memory, and the DMI memory backs up the BIOS
4 settings.